** NATIONAL UNIVERSITY OF COMPUTER & EMERGING SCIENCES**

**PROJECT:**  
 DIGITAL LOGIC DESIGN

**TOPIC:**

4 BIT COUNTER D FLIP FLOP

**GROUP MEMBERS:**

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**Working Software:** We can make our circuit in soft form on software (**Logisim**).

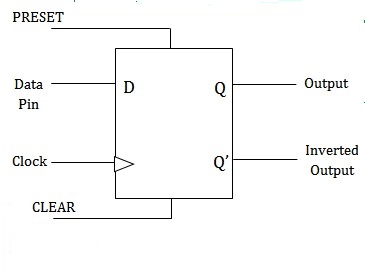
**Link for Download Logisim Software :**

[**https://sourceforge.net/projects/circuit/**](https://sourceforge.net/projects/circuit/)

**Definition:**

A 4-bit **synchronous counter** built from D-flipflops with carry-input and carry-output. In this circuit, the single clock signal is directly connected to all flipflops, so that all flipflops change state at the same time.

**D-Flip Flop:**

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**Table:**

|  |  |  |
| --- | --- | --- |
| Pin | Input/Output | Description |
| D | Input | Data input |
| CLK | Input | Clock input |
| Q<3:0 | Output(4-bits) | Count Output |

**Explanation:**

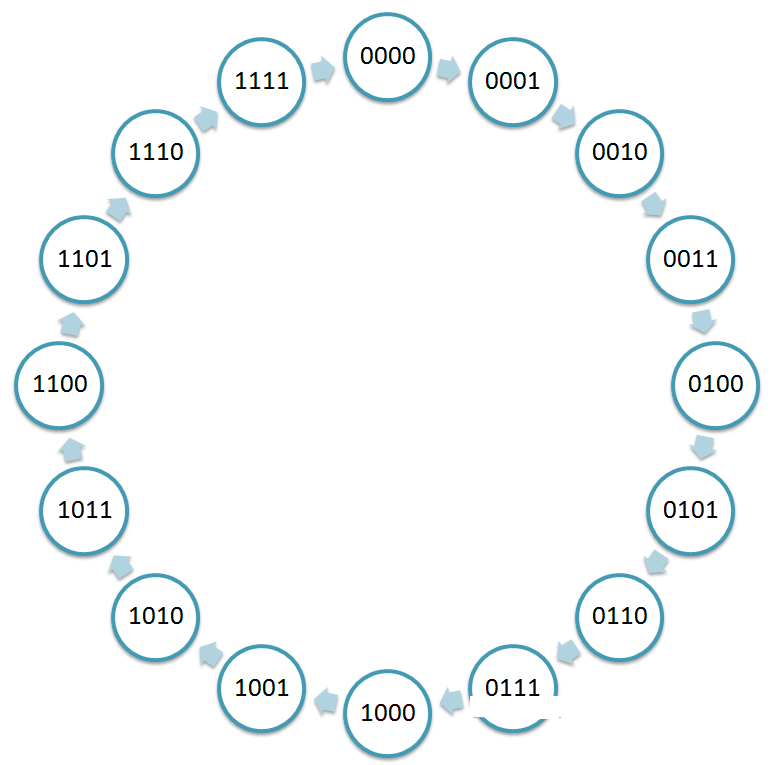
A 4-bit **synchronous counter** built from D-flipflops with carry-input (count-enable) and carry-output. In this circuit, the single clock signal is directly connected to all flipflops, so that all flipflops change state at the same time. It consists of:

* 4 Ex-OR gates.
* 4 OR gates.
* 6 AND gates.
* 1 NOT gate.
* 1 Clock.
* Set/Reset State.
* Up/down.

In this circuit, the input of **D-flipflop** is connected with the **clock** and data pin of **D-filpflop** is connected with the output of the **ex-or gate** and the bottom part of **D-filpflop** which is actually known as “**clear**”is connected with the reset button.The output part of **D-flipflop** is connected with four pins from which we can observed that our 4 bit counter is in set state or reset state. The output of **or gates** is connected with the second input of **ex or gate**. The first input of **ex-or gate** is connected with the second input of second and gate. **Not gate** is short circuit by up and down button. The output of two and gates is connected with input of **or gate**.

**Excitation table for D-Flipflop:**

|  |  |  |
| --- | --- | --- |
| Present State  (Q) | Input (D) | Next State  (Q+) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

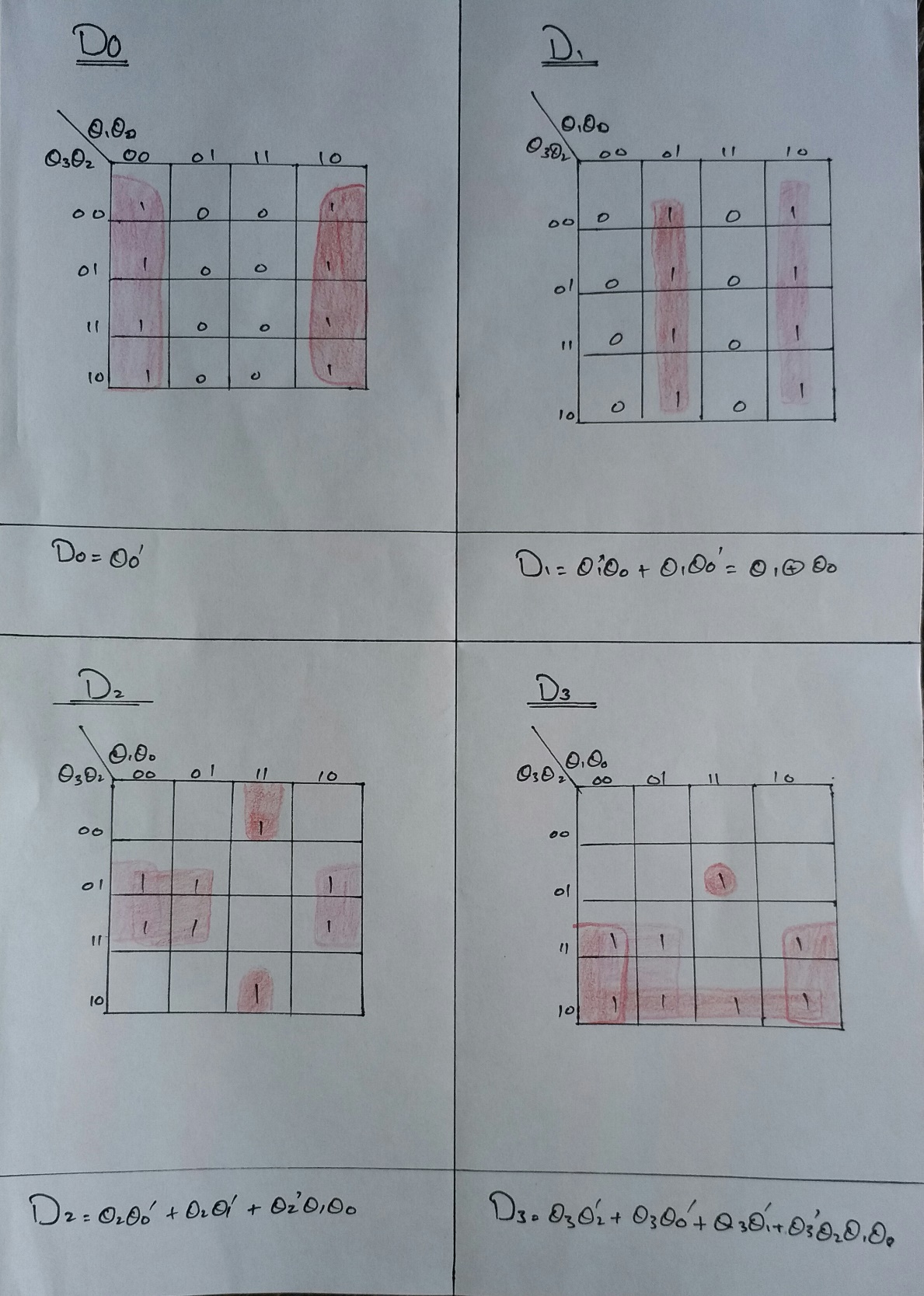
**State Diagram of bit counter:**

**Truth Table of 4 bit counter:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Present State  (Q3 Q2 Q1 Q0) | Next State  (Q3+ Q2+ Q1+ Q0+) | D3 | D2 | D1 | D0 |
| 0000 | 0001 | 0 | 0 | 0 | 1 |
| 0001 | 0010 | 0 | 0 | 1 | 0 |
| 0010 | 0011 | 0 | 0 | 1 | 1 |
| 0011 | 0100 | 0 | 1 | 0 | 0 |
| 0100 | 0101 | 0 | 1 | 0 | 1 |
| 0101 | 0110 | 0 | 1 | 1 | 0 |
| 0110 | 0111 | 0 | 1 | 1 | 1 |
| 0111 | 1000 | 1 | 0 | 0 | 0 |
| 1000 | 1001 | 1 | 0 | 0 | 1 |
| 1001 | 1010 | 1 | 0 | 1 | 0 |
| 1010 | 1011 | 1 | 0 | 1 | 1 |
| 1011 | 1100 | 1 | 1 | 0 | 0 |
| 1100 | 1101 | 1 | 1 | 0 | 1 |
| 1101 | 1110 | 1 | 1 | 1 | 0 |
| 1110 | 1111 | 1 | 1 | 1 | 1 |
| 1111 | 0000 | 0 | 0 | 0 | 0 |

**K –Map:**

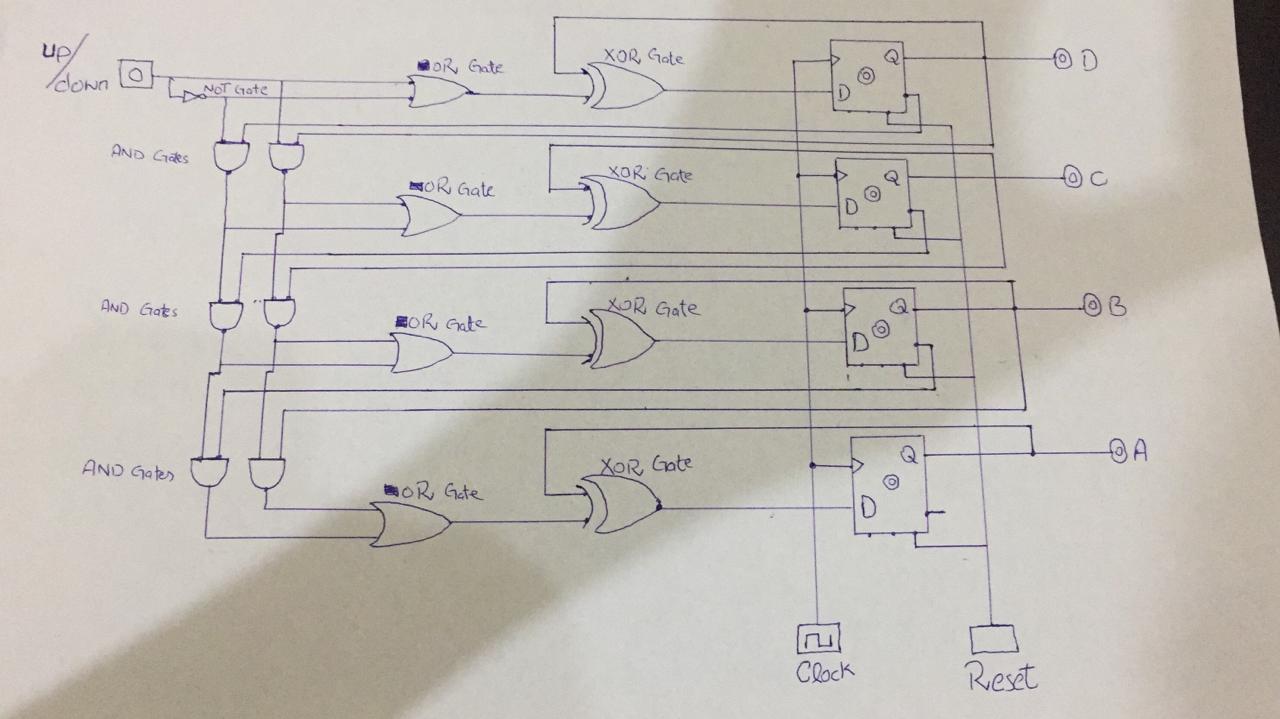
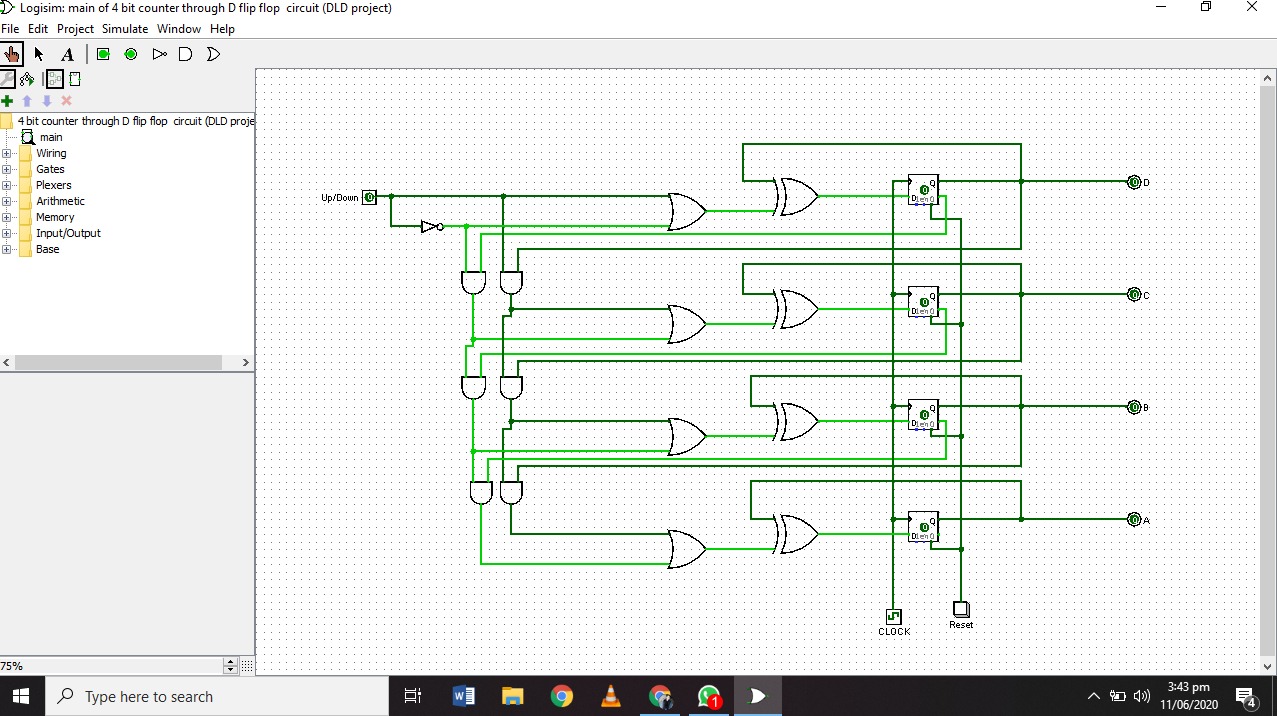
Now we use the k-map to find out the logic expressions D0, D1, D2 and D3.



So, we found the value of D3, D2, D1, D0 in terms of Q3, Q2, Q1.

**Circuit Diagram:**

Following is the paper work of the circuit:

Circuit Diagram: